Institute for Nuclear Research



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The T2K experiment



The Near Detector upgrade



The SuperFGD detector



The T2K (Tokai-to-Kamioka) experiment is a long baseline neutrino oscillation experiment designed to probe the mixing of the muon neutrino (antineutrino) with other species and shed light on the neutrino mass scale. reconstruct the energy of the neutrino or antineutrino based on measurements of the resultant visible particles from the neutrino interaction.

Physics goals:

Measurement of the neutrino oscillation parameters with precision of $\delta(\Delta m^2_{23}) \sim 10^{-4} \text{eV}^2$ and $\delta(\sin^2 2\theta_{23}) \sim 0.01$ via ν_{μ} disappearance studies. Search for CP violation in the lepton sector.



CAD 3D Model of the ND280 upgrade detector. In the upstream part (on the left in the drawing) two High-Angle TPCs (brown) with the scintillator detector Super-FGD (gray) in the middle.

The upgraded ND280 detector will be able to perform a full exclusive reconstruction of the final state from neutrino-nucleus interactions.

- Measurements of low momentum protons and pions and for the first time, event-by event measurements of neutron kinematics
- 4π acceptance for muons
- Decrease systematic uncertainties to 3-4% (from current 6-7%)
- Separation of electrons and gamma radiation

The SuperFGD detector will be an important part of the ND280 near detector upgrade for both the T2K and Hyper-Kamiokande projects.

- The dimension of the active part of SuperFGD is $192 \times 56 \times 182$ cm3, ~56000 of readout channels.
- The scintillator cubes are produced at UNIPLAST Co. (Vladimir, Russia), comsist of polystyrene doped with 1.5% of paraterphenyl (PTP) and 0.01% of POPOP. Size: 1.0× 1.0× 1.0 cm3
- WLS fibers are commonly used to collect light from large area of scintillators, produced by Kuraray Co Y-11, shape type fiber with 1.0 mm diameter

SFGD electronics









The SuperFGD electronics consist of 16 crates. One crate is an Optical Concentrator Board (OCB) in the middle of the crate section for initial data aggregation, Backplane, 14 Front End Boards (FEB) for analog processing, ADC, bias voltage to the MPPCs. Each crate is connected to the Master Clock Board (MCB), which provides a common clock signal and synchronization. The FEB architecture is based on 8 CITIROC chips that can each read signals from 32 MPPCs, one FPGA Altera Aria X to control, and manage the timing and data flow from the CITIROCs, one 8-channel ADC for the digitization of the CITIROC analog output.

The signal from MPPC goes to CITIROC, which provides a measurement of amplitude, the HG and LG signal paths, whose output from the CITIROC is digitized by a 12-bit ADC and the Time over Threshold (ToT) obtained by sampling the rising and falling edges of the CITIROC trigger lines at 400 MHz by the FPGA on the FEB.

Baseline scan	HG/LG vs ToT calibration	HG calibration
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	The separation of the signal into HG and LG allows to generate a signal amplitude with a large dynamic range and small accuracy or with high accuracy and a small dynamic range.	Gain_distribution Star 2 128.278068 +/- 0.104807 mean peak 2 = 128.278068 +/- 0.104807 mean peak 3 = 171.729520 +/- 0.140020 mean peak 4 = 218.082951 +/- 0.202802 mean peak 5 = 263.020205 +/- 0.411446 gain = 44.914046 +/- 0.289322